each pixel includes a barrier region disposed under said refractory metal and a storage region adjacent said barrier region, said [sad] storage region including N-type dopant implanted into at least elements (e) through (i).

26. (Amended) A semiconductor imaging device, comprising:

a plurality of pixels formed from a multilayer sandwich including

a substrate,

a collector ohmic contact layer disposed above said substrate,

a gate ohmic contact layer disposed above said substrate,

at least one modulation doped quantum well heterostructure disposed above said substrate between said collector ohmic contact layer and said gate ohmic contact layer, wherein said modulation doped quantum well heterostructure includes at least one quantum well structure, a modulation doped layer and an undoped spacer layer disposed between said at least one quantum well structure and said modulation doped layer;

an undoped spacer layer, a charge source layer, and a cladding layer disposed above said substrate between said modulation doped quantum well heterostructure and said gate ohmic contact layer;

each pixel including

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a gate metal layer formed on a portion of said gate ohmic contact layer for said pixel,

a barrier region disposed under said gate metal layer,

a storage region adjacent said barrier region, said storage region including dopant implanted into portions of said multilayer sandwich [at] between said charge source layer and said modulation doped quantum well heterostructure.

Clean Set of Claims

Below is a clean set of claims as amended by the amendment presented above.

9. A semiconductor imaging device, comprising:

a) a semiinsulating gallium arsenide (GaAs) substrate;

b) a distributed Bragg reflector mirror epitaxially grown on said semiinsulating GaAs substrate;

c) a first layer of P+ type GaAs deposited on said distributed Bragg reflector mirror for contacting a collector electrode;

d) at least one layer of aluminum gallium arsenide (AlGaAs) disposed on said first layer of P+ type GaAs;

e) an epitaxial layer structure of at least one quantum well of InGaAs having GaAs layers on each either side;

f) a first spacer layer of AlGaAs disposed on said epitaxial layer structure;

g) an N type modulation doped layer of AlGaAs disposed on said first spacer layer;

h) a second spacer layer of AlGaAs disposed on said modulation doped layer;

i) a planar doped layer of P+ type AlGaAs disposed on said second spacer layer;

j) a cladding layer of AlGaAs of modest P type doping disposed on said planar doped layer; and

k) a layer of GaAs of P++ type doping disposed on said cladding layer for contacting a gate electrode,

wherein a forward bias is applied to said gate electrode with respect to said collector electrode such that light incident on said semiconductor imaging device causes charge to leave said at least one quantum well.

10. A semiconductor imaging device according to claim 9, wherein:

said at least one quantum well comprises two or three quantum wells, adjacent of said two or three quantum wells being separated by a GaAs layer.

11. A semiconductor imaging device according to claim 9, wherein:

said at least one layer of aluminum gallium arsenide (AlGaAs) comprises a P type AlGaAs layer disposed on said first layer of P+

type GaAs and a first layer of undoped AlGaAs disposed on said P type AlGaAs layer.

12. A semiconductor imaging device according to claim 11, wherein:

said at least one layer of aluminum gallium arsenide further comprises a second layer of undoped AlGaAs disposed on said first layer of undoped AlGaAs, said first layer of undoped AlGaAs having a first aluminum content, and said second layer of undoped AlGaAs having a second aluminum content smaller than said first aluminum content.

13. A semiconductor imaging device according to claim 12, wherein:

said first aluminum content is greater than 40% and less than 100%, and said second aluminum content is greater than 10% and less than 30%.

14. A semiconductor imaging device according to claim 13, wherein:

said first aluminum content is approximately 70% and said second aluminum content is approximately 15%.

15. A semiconductor imaging device according to claim 13, further comprising:

a refractory metal disposed on a portion of said layer of GaAs of P++ type doping, said refractory metal adapted to receive a voltage.

16. A semiconductor imaging device according to claim 9, wherein:

said semiconductor imaging device is arranged as a pixel with elements j) and k) constituting a mesa extending a first horizontal distance, and elements a) through i) extending a second horizontal distance larger than said first horizontal distance.

17. A semiconductor imaging device according to claim 16, further comprising:

a refractory metal disposed on a portion of said mesa layer of GaAs of P++ type doping, said refractory metal adapted to receive a voltage.

18. A semiconductor imaging device according to claim 9, wherein:

said semiconductor imaging device is arranged as a plurality of pixels, each of said plurality of pixels having a mesa formed from elements j) and k) and separated from an adjacent mesa by a transfer region which does not include elements j) and k) and which is implanted with N+ type doping to form a low resistance path between adjacent mesas.

19. A semiconductor imaging device according to claim 18, further comprising:

a refractory metal disposed on a portion of each said mesa atop a layer of GaAs of P++ type doping, said refractory metal adapted to receive a voltage.

20. A semiconductor imaging device according to claim 19, further comprising:

a charge sensitive amplifier coupled to one of said plurality of pixels.

21. A semiconductor imaging device according to claim 20, wherein:

said plurality of pixels comprise a linear array of pixels, said one of said plurality of pixels to which said charge sensitive amplifier is coupled being a last pixel in said linear array, and said charge sensitive amplifier and said linear array together comprise a charge coupled device wherein said plurality of pixels store charges, and wherein said charges are transferred from one pixel to another by an application of clocked voltages to said refractory metal disposed on said mesas.

23. A semiconductor imaging device according to claim 22, wherein:

said array of pixels is controlled by a 1 1/2 phase clocking scheme, and every other pixel in said linear array of pixels is biased to a constant voltage, and the remaining pixels are clocked with a single phase clock.

24. A semiconductor imaging device according to claim 19, further comprising:

a plurality of charge sensitive amplifiers respectively coupled to individuals of said plurality of pixels to generate a plurality of analog signals corresponding to charge that leaves said plurality of pixels during an imaging cycle.

25. A semiconductor imaging device according to claim 19, wherein:

each pixel includes a barrier region disposed under said refractory metal and a storage region adjacent said barrier region, said storage region including N-type dopant implanted into at least elements (e) through (i).

26. A semiconductor imaging device, comprising:

a plurality of pixels formed from a multilayer sandwich including

a substrate,

a collector ohmic contact layer disposed above said substrate,

a gate ohmic contact layer disposed above said substrate,

at least one modulation doped quantum well heterostructure disposed above said substrate between said collector ohmic contact layer and said gate ohmic contact layer, wherein said modulation doped quantum well heterostructure includes at least one quantum well structure, a modulation doped layer and an undoped spacer layer disposed between said at least one quantum well structure and said modulation doped layer;

an undoped spacer layer, a charge source layer, and a cladding layer disposed above said substrate between said modulation doped quantum well heterostructure and said gate ohmic contact layer;

each pixel including

a gate metal layer formed on a portion of said gate ohmic contact layer for said pixel,

a barrier region disposed under said gate metal layer,

a storage region adjacent said barrier region, said storage region including dopant implanted into portions of said multilayer sandwich between said charge source layer and said modulation doped quantum well heterostructure.

27. A semiconductor imaging device according to claim 26, wherein a forward bias is applied to said gate metal layer electrode with respect to said collector contact layer for a given

pixel such that incident light causes charge to leave said modulation doped quantum well heterostructure of the given pixel.

29. A semiconductor imaging device according to claim 26, wherein:

transfer regions, each disposed between a pixel pair and formed from said multilayer sandwich with the gate ohmic contact layer and cladding layer removed, and which is implanted with dopant to form a low resistance path between adjacent pixels.

30. A semiconductor imaging device according to claim 29, wherein:

said plurality of pixels store charges that are transferred from one pixel to another via said transfer regions by an application of clocked voltages to said gate metal layers of said pixels.

31. A semiconductor imaging device according to claim 30, wherein:

said plurality of pixels are logically arranged in a linear row that includes a last pixel, and a charge sensitive amplifier is coupled to said last pixel to generate an analog signal corresponding to charge supplied thereto.

32. A semiconductor imaging device according to claim 26, wherein:

said modulation doped quantum well heterostructure comprises at least one undoped quantum well structure designed for intersubband absorption.

33. A semiconductor imaging device according to claim 32, wherein:

said modulation doped quantum well heterostructure comprises a modulation doped layer of N+ type material.

34. A semiconductor imaging device of according to claim 33, wherein:

said charge source layer comprises a thin layer of P+ type material.

35. A semiconductor imaging device of according to claim 33, wherein:

said cladding layer comprises a layer of P type material.

36. A semiconductor imaging device according to claim 26, wherein:

said multilayer sandwich is substantially formed from group III-V materials.